

REMARKS/ARGUMENTS

Claims 1-15 and 17-20 are pending in this application, the allowability of the claims having been withdrawn in view of the newly discovered reference to Hidaka (US Patent No. 6,635,934). Claims 1, 5, 8, 11, 14, 17, and 19 are amended. New claims 21-27 are presented for examination.

Claims 1-15 and 17-20 stand rejected under 35 USC 102(e) as being anticipated by Hidaka. The rejection of these claims, as now amended, is respectfully traversed.

Hidaka teaches an internal circuit node voltage V_{ccs} , which is clearly shown in FIG. 19. The actual power supply is V_{cc} , which is a normal external power supply having a substantially constant voltage level, and is not generated by the circuit itself. In contrast, the internal voltage, V_{ccs} , is generated by a P-channel transistor, which is in turn switched by the gate voltage signal designated " Φ ". In effect, the internal voltage V_{ccs} is merely an internal signal node or a power-gated supply line with a varying voltage signal. Evidence of this is given in the immediately adjacent timing diagram of FIG. 20, in which V_{ccs} is shown to be a switched signal and not a "supply voltage source" as claimed.

However, in a spirit of cooperation and to obtain the allowance of claims 1-15 and 17-20, each of the independent claims 1, 5, 8, 11, 14, 17, and 19 have been further restricted so that the supply voltage source cannot be more broadly interpreted than was originally intended. Each of the independent claims has been amended to recite that the supply voltage source provides a "substantially constant" power supply voltage and not a switched internal circuit signal or gated power supply voltage as taught in Hidaka. No new matter has been introduced into the independent claims, since the originally intended meaning of the claim term in question is now made explicit. Similarly, independent claims 1, 5, 8, 11, 14, 17, and 19 have been amended to claim a "substantially constant" reference

voltage source to prevent the reference voltage source from being more broadly interpreted than was originally intended. No new matter is deemed to have been added by this amendment.

Claims 1, 5, 8, 11, 14, 17, and 19, therefore, are deemed to be allowable as containing a limitation not taught in the Hidaka reference. The remaining claims are deemed to be allowable as being dependent from an allowable base claim for the reasons given above.

New claims 21-27 are deemed to be allowable as being dependent upon a respective allowable base claim. No new matter is deemed to be added by new claims 21-27. Claims 21-27 are deemed to be fully supported by an inspection of drawing FIG. 2 of the present application.

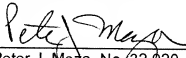
The present invention, as claimed, is deemed to be an advance over the circuit to Hidaka, and other similar circuits because of the speed advantages obtained due to the direct coupling of the output stage transistors between VCC and ground. The attendant advantages of this structure are explained, *inter alia*, in the specification at page 9, lines 12-32.

In view of all of the above, claims 1-15 and 17-27 are now believed to be allowable and the case in condition for allowance which action is respectfully requested. Should the Examiner be of the opinion that a telephone conference would expedite the prosecution of this case, the Examiner is requested to contact Applicants' attorney at the telephone number listed below.

Please charge deposit account no. 50-1123 \$350 to cover the fee for claims in excess of 20 claims (i.e., 7 claims in excess of the 20 claims previously paid for). No additional fee is believed due for this submittal. However, any fee deficiency associated with this submittal may be charged to Deposit Account No. 50-1123.

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Respectfully submitted,



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